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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,127	12/11/2003	Chen-Chi Kuo	P17480	7873

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EXAMINER	
CHRISS, ANDREW W	

ART UNIT	PAPER NUMBER
2619	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,127	KUO ET AL.	
	Examiner	Art Unit	
	Andrew Chriss	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 2, 4-13, and 14-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 4-13, and 14-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment, filed October 12, 2007, is acknowledged and has been entered. Claims 1, 4, 12, 15, 22, and 24 are amended, claims 3 and 14 are canceled, and claims 1, 2, 4-13, and 14-25 are currently pending.

Claim Objections

2. **Claims 1, 12, 22, 24, and 25** objected to because of the following informalities:

Regarding Claims 1, 12, 22, and 24, claim language "...each interface availability indicator being associated with one of a plurality interfaces" should be modified to read "...each interface availability indicator being associated with one of a plurality *of* interfaces". Appropriate correction is required.

Regarding Claim 25, claim language "(Original)" should be removed from the end of the claim.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claims 22 and 24** rejected under 35 U.S.C. 102(e) as being anticipated by Kramer et al (United States Patent Application Publication US 2003/0161291 A1), hereinafter Kramer.

Regarding Claim 22, Kramer teaches a network processor 102 that stores at least part of a time slot table (equivalent to Applicant's claimed calendar structure) on an internal memory.

An exemplary time slot table structure is shown in Figure 4, wherein each location in the table stores multiple scheduled transmission element identifiers (paragraph 0039). The transmission elements linked to a given element that has its identifier stored in the first portion of a given time slot table location may be referred to as being in a dynamic "waiting room," i.e., awaiting selection for transmission (paragraph 0047). Further, the time slot tables "may also be stored at least in part in the external memory of the network processor" (paragraph 0036), and further shown in Figure 2, thus teaching an apparatus containing a processor locally storing a first portion of a calendar structure and an external memory to store a second portion of a calendar structure. The apparatus "may comprise a router or switch which includes multiple line cards" (paragraph 0024) and that "each of the tables in a set of tables may be associated with a particular interface or other network connection," (paragraph 0037) thus providing a calendar structure associated with a plurality of interfaces. Further, "time slot tables include a plurality of locations, each corresponding...to a transmission time slot" (paragraph 0037), thus denoting a series of entries associated with time periods. A set of pointers is associated with each of the entries that track the actual transmission time through the table and denote a "waiting room" for data blocks (paragraphs 0049-0051), and thus correspond to interface availability indicators. As the pointer values provide an indication of when a transmission time slot will become available, being constantly updated as data blocks move through the table (paragraphs 0052-0054), the therefore indicate when the interface will transition to become available.

Regarding Claim 24, Kramer teaches a processing element to locally store a first portion of a calendar structure, an external memory storing a second portion of a calendar structure, and the claimed calendar structure features as described with regards to Claim 22 above. Further,

Kramer teaches a switch fabric (Figure 1, 110) connected to the network processor (Figure 1, 102). The invention is capable of use in an ATM network (paragraph 0069), thus teaching an ATM switch fabric.

Claim Rejections - 35 USC § 103

5. **Claims 1-4, 12-15, 23, and 25** rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer in view of Manning et al (United States Patent 5,862,137), hereinafter Manning.

Regarding Claim 1, Kramer teaches a network processor 102 that determines an interface has become available based on an entry in a time slot table, which is stored at least in part in the internal memory of the network processor and at least in part in an external memory, as described with regards to Claim 22 above. However, Kramer does not teach updating a location in a shaper vector to indicate that the interface is now available to transmit packets, wherein the shaper vector includes locations associated with a plurality of interfaces. In the same field of endeavor, Manning teaches a bit vector (equivalent to Applicant's claimed shaper vector), which includes eight bits, each bit corresponding to a specific output port (column 4, lines 37-39). Further, Manning teaches that "the cell will be transmitted when a dynamic bandwidth opportunity becomes available for simultaneous transmission to each output port designated by the request" (column 4, lines 52-55). According to Manning's invention, a location in the bit vector corresponding to the requested output port would need to be updated prior to transmission. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the bit vector taught in Manning with the time slot table (calendar

structure) taught in Kramer in order to facilitate point-to-multipoint transmission by reducing or eliminating delays and cell loss (column 1, lines 46-48).

Regarding Claim 2, Manning further teaches that the bit vector contains a series of eight bits, and indicates designated output ports for transmission. A logic value of "1" indicates that a port is requested, thus busy; whereas a logic value of "0" indicates the port is available to transmit packets. Based on this information, the bandwidth arbiter 12 will generate an unassigned output port bit vector, which is updated based on information in the requested bit vector and all allocated bit vectors, and toggling *each resultant bit* to provide a single unassigned output port bit vector (column 55-61), thus updating an appropriate bit in the shaper vector. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Manning with Kramer in order to facilitate point-to-multipoint transmission by reducing or eliminating delays and cell loss (column 1, lines 46-48).

Regarding Claim 4, Manning further teaches using an OR operation to combine all allocated bit vectors from a switch allocation table (equivalent to Applicant's claimed first portion of a calendar structure) with a requested bit vector (equivalent to Applicant's claimed shaper vector) to generate an unassigned output port bit vector (column 4, lines 55-61). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Manning with Kramer in order to facilitate point-to-multipoint transmission by reducing or eliminating delays and cell loss (column 1, lines 46-48).

Regarding Claim 12, Kramer teaches "an article of manufacture comprising a computer-readable storage medium for use in conjunction with a processor, the medium storing one or

more software programs" (page 7, Claim 20) which, in combination with the teachings of Manning as described with regards to Claim 1 above, perform the claimed steps.

Regarding Claim 13, see rejection of Claim 2 above.

Regarding Claim 15, see rejection of Claim 4 above.

Regarding Claim 23, Kramer teaches all of the limitations of Claim 22, as described above. However, Kramer does not teach a processor element locally storing a shaper vector indicating which interfaces are currently available to transmit packets. In the same field of endeavor, Manning teaches a bandwidth arbiter 12 that locally stores bit vectors (equivalent to Applicant's claimed shaper vector), which indicates which interfaces are currently available to transmit packets (column 4, lines 37-39). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the bit vector taught in Manning with time slot table (calendar structure) taught in Kramer in order to facilitate point-to-multipoint transmission by reducing or eliminating delays and cell loss (column 1, lines 46-48).

Regarding Claim 25, see rejection of Claim 23 above.

6. **Claims 5, 6, 16, and 17** rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer in view of Manning as applied to claims 1 and 12 above, and further in view of Yu et al (United States Patent 7,031,305), hereinafter Yu.

Regarding Claim 5, Kramer and Manning teach all of the limitations of Claim 1, as described above. However, the references do not teach pre-fetching a subset of the second portion of the calendar structure from the external memory and locally storing the subset at the processing element as the first portion. In the same field of endeavor, Yu teaches a scheduler 80 directly fetching an assignment table (equivalent to Applicant's claimed second portion of a

calendar structure) from the programmable memory device 102 (memory external to a processing element) and written into internal registers of the network switch 12, thus locally storing a subset of the fetched table. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Yu with Kramer, as modified by Manning above, in order to assign memory access slots according to a programmable memory slot assignment scheme to avoid waste of bandwidth resources (column 1, lines 65-67).

Regarding Claim 6, Kramer, Manning, and Yu teach all of the limitations of Claim 5 above. Further, Manning teaches using an OR operation to combine retrieved information and storing the result as a first part of a calendar structure. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Manning with Kramer in order to facilitate point-to-multipoint transmission by reducing or eliminating delays and cell loss (column 1, lines 46-48). However, Kramer and Manning do not teach clearing the first portion of the calendar structure, or retrieving the subset of the second portion from the external memory. In the same field of endeavor, Yu teaches changing information in an assignment table memory, thus clearing the first portion of a calendar structure. Further, Yu teaches retrieving a subset of an assignment table from an external programmable memory device. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Yu with Kramer, as modified by Manning above, in order to assign memory access slots according to a programmable memory slot assignment scheme to avoid waste of bandwidth resources (column 1, lines 65-67).

Regarding Claim 16, see rejection of Claim 5 above.

Regarding Claim 17, see rejection of Claim 6 above.

7. **Claims 7-9, 11, and 18-20** rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer in view of Manning as applied to claims 1 and 12 above, and further in view of Kikuchi et al (United States Patent 7,120,125), hereinafter Kikuchi.

Regarding Claim 7, Kramer and Manning teach all of the limitations of Claim 1 above. Kramer teaches enqueuing and dequeuing packets to be transmitted via a plurality of ports, thus determining packets to be transmitted via any one of the ports. Manning teaches updating a location in the shaper vector to indicate that the first interface is not available, via the combination of the stored allocation tables and the bit vector to make an unassigned port bit vector (column 5, lines 1-4). In addition, Manning teaches updating an entry in a calendar structure to indicate when the interface will again become available, via the generated unassigned port bit vector table. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Manning with Kramer in order to facilitate point-to-multipoint transmission by reducing or eliminating delays and cell loss (column 1, lines 46-48). However, the references do not teach calculating a time when the first interface will again be available. In the same field of endeavor, Kikuchi teaches calculating a queuing delay factor, which corresponds to a time when the first interface will again be available (column 22, lines 8-13). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Kikuchi with Kramer, as modified above, in order to monitor performance of file transfers using protocols sensitive to start and stop times, such as Hypertext Transfer Protocol (HTTP) and File Transfer Protocol (FTP).

Regarding Claim 8, Manning further teaches selecting an interface based on information stored in a bit vector. In the example, the interfaces (2,3) are requested and are assigned based

on the information stored within the bandwidth arbiter. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Manning with Kramer, as modified above, in order to facilitate point-to-multipoint transmission by reducing or eliminating delays and cell loss (column 1, lines 46-48).

Regarding Claim 9, Kikuchi further teaches that the queuing delay factor "increases by the amount obtained by dividing the size S of the packet by a transmission rate B of the link" (column 22, lines 16-18). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Kikuchi with Kramer, as modified above, in order to monitor performance of file transfers using protocols sensitive to start and stop times, such as HTTP and FTP.

Regarding Claim 11, Manning teaches a bandwidth arbiter which performs the functions of Applicant's claimed transmission block and timer blocks. With regards to the functions performed by the transmission block, Manning teaches the bandwidth arbiter determining a packet (cell) to be transmitted (column 3, lines 12-13), updating the shaper vector to indicate that the first interface is not available, and updating the calendar structure (column 5, lines 1-4). With regards to the functions performed by the timer block, Manning teaches the bandwidth arbiter determines that an interface has become available to transmit packets based on an entry in a first portion of a calendar structure and updates the shaper vector to indicate that the interface is now available (column 4, lines 66-67).

Regarding Claim 18, see rejection of Claim 7 above.

Regarding Claim 19, see rejection of Claim 8 above.

Regarding Claim 20, see rejection of Claim 9 above.

8. **Claims 10 and 21** rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer in view of Manning and Kikuchi, as applied to claims 7 and 18 above, and further in view of Ganesh et al (United States Patent Application Publication US 2002/0051450 A1), hereinafter Ganesh.

Regarding Claim 10, Kramer, Manning, and Kikuchi teach all of the limitations of Claim 7 above. However, the references do not teach determining whether an entry of a calendar structure to be updated is stored in the first portion of the calendar structure. In the same field of endeavor, Ganesh teaches a switching device containing multiple ports, each of which has a lookup table containing network address information and an age field relating to how recently the associated network address has been used (paragraph 0020), thus equivalent to Applicant's calendar structure. Further, Ganesh teaches that a search engine searches memory to determine whether a destination address read from a network frame is located within the lookup table of memory (paragraph 0029; Figure 4), thus determining whether an entry to be updated is located in a first part of a calendar structure. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Ganesh with Kramer, as modified above, in order to efficiently store address lookup table entries, saving memory space by only storing addresses used by a particular port.

Regarding Claim 21, see rejection of Claim 10.

Response to Arguments

9. Applicant's arguments filed October 12, 2007 have been fully considered but they are not persuasive. Applicant alleges the Kramer reference fails to teach entry rows associated with time periods, wherein each entry row includes dedicated interface availability indicators and each interface availability indicator shows if a particular interface will transition to become available. However, Kramer, as discussed with regards to Claim 22 and cited in the rejections for Claims 1, 12, and 24, discloses a set of pointers is associated with each of the entries that track the actual transmission time through the table and denote a "waiting room" for data blocks (paragraphs 0049-0051), and thus correspond to interface availability indicators. As the pointer values provide an indication of when a transmission time slot will become available, being constantly updated as data blocks move through the table (paragraphs 0052-0054), the therefore indicate when the interface will transition to become available. Therefore, rejection of Claim 22 under 35 U.S.C. 102(e) is maintained. Further, rejection of Claims 1, 12, and 24 under 35 U.S.C. 103(a) is also maintained.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Manning et al (United States Patent 5,982,776) is directed to multipoint-to-point arbitration in a network switch.

b. Bonomi et al (United States Patent 6,011,775 and United States Patent 6,349,089) is directed to a method and apparatus for integrated traffic shaping in a packet-switched network, and flexible scheduling in an ATM switch.

c. Gritton (United States Patent 5,940,397) is directed to methods and an apparatus for scheduling ATM cells.

d. Reynolds (United States Patent 6,768,717) is directed to an apparatus and method for traffic shaping in a network switch.

e. Beshai et al (United States Patent Application Publication US 2007/0171900 A1) is directed to data burst scheduling.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Chriss whose telephone number is 571-272-1774. The examiner can normally be reached on Monday - Friday, 7:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew Chriss
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AC

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